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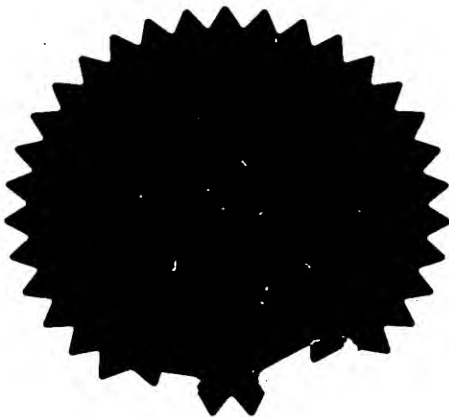
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1. Your reference

P015271GB

13 JAN 2003

2. Patent application number

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0300710.1

3. Full name, address and postcode of the or of each applicant (*underline all surnames*)

ARM Limited
110 Fulbourn Road
Cherry Hinton
Cambridge
CB1 9NJ

Patents ADP number (*if you know it*)

7498124002

If the applicant is a corporate body, give the country/state of its incorporation

United Kingdom

4. Title of the invention

Data Processing Performance Control

5. Name of your agent (*if you have one*)

D Young & Co

"Address for service" in the United Kingdom to which all correspondence should be sent (*including the postcode*)

21 New Fetter Lane
London
EC4A 1DA

Patents ADP number (*if you know it*)

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Abstract 1

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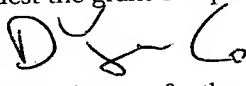
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Statement of inventorship and right to grant of a patent (Patents Form 7/77) 2

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11. I/We request the grant of a patent on the basis of this application.
Signature  Date 13 January 2003
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12. Name and daytime telephone number of person to contact in the United Kingdom Nigel Robinson 023 8071 9500

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**Statement of inventorship and of
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13 JAN 2003

1. Your reference
P015271GB

2. Patent application number
(if you know it)

3. Full name of the or of each applicant
ARM Limited

0300710.1

4. Title of the invention
Data Processing Performance Control

5. State how the applicant(s) derived the right
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DY & Co

Date 13 January 2003

D Young & Co (Agents for the Applicants)

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Nigel Robinson

023 8071 9500

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DATA PROCESSING PERFORMANCE CONTROL

This invention relates to the field of data processing systems. More particularly, this invention relates to the field of the control of data processing performance, such as, for example, so as to reduce the energy consumed by a data processing system.

An important consideration in data processing systems is their energy consumption. Data processing systems which consume less energy allow longer battery life in mobile devices, tend to run cooler and more reliably, and require fewer special engineering considerations to deal with heat dissipation and the like. It is strongly desirable to reduce the energy consumption of data processing systems.

Balanced against a desire to reduce the energy consumption of data processing systems is a simultaneous desire to increase their performance level to deal with increasingly computationally intensive tasks. Such tasks often require highly intensive processing operations for short periods of time followed by relatively long idle times in which little computation is required.

In order to address the above two factors, it is known to produce data processing systems that are able to change their performance level so that high computational performance is provided in some configurations and low energy consumptions in other configurations. Known systems, such as the LongRun software produced by Transmeta, or the SpeedStep systems produced by Intel, allow a processor to be switched between such different configurations. In order to match the desired performance goals, a high computational performance configuration would be one with a relatively high operating voltage and a relatively high processor clock frequency. Conversely, a low energy consumption configuration has a relatively low operating voltage and a relatively low processor clock frequency.

As well as providing the performance and energy management capabilities described above, another important design characteristic is that hardware and software designs should be re-useable in a relatively large number of different circumstances. If computer software, such as operating system software, has to be re-written for

different hardware implementations, or the hardware designs significantly modified for different hardware implementations, then this is strongly disadvantageous.

Viewed from one aspect the present invention provides apparatus for processing data, said apparatus comprising:

a processor operable to perform data processing operations under control of program instructions, said processor being operable under program instruction control to generate a performance level request signal indicative of a desired data processing performance level of said processor; and

a mapping circuit operable to map said performance level request signal into a control signal supplied to one or more further circuits to control operation of said one or more further circuits so as to support said desired data processing performance level of said processor such that said program instructions controlling generation of said performance level request signal are independent of how said one or more further circuits are controlled to meet said desired data processing performance level.

The present invention recognises that significant advantages arise by providing a layer of abstraction between desired data processing performance levels set under software control and the control signals generated to manipulate the associated hardware elements to match the performance requirement. This layer of abstraction with its associated required mapping runs counter to the technical prejudice in the field which is to allow the software to directly control the hardware. The present technique recognises that providing an abstraction and associated mapping between the desired data processing performance levels set by the software and the control signals generated allows reuse of the same software on different hardware platforms with the differences being dealt with by the mapping. Furthermore, the hardware platform can be modified, such as by the provision of more or fewer performance management capabilities, with corresponding necessary changes being substantially confined to the mapping arrangement.

It will be appreciated that the further circuits which can be controlled in dependence upon the desired processing performance level could take a wide variety of different forms. Particularly preferred embodiments utilise further circuits being clock generators and voltage controllers. The clock signal frequency and the supply

voltage have a strong affect upon energy consumption. It would however be possible for the further circuits to take other forms such as, for example, cache memories. The cache memories could be enabled or disabled without functionally changing the program operation.

5

In preferred embodiments of the invention the control signals into which the desired data processing performance level is mapped are thermometer coded. Such thermometer coding provides an advantageous degree of resistance to transient effects that may occur due to sampling of values across clock boundaries; in such systems
10 signal transfers across clock boundaries are relatively common.

Furthermore, thermometer coding whilst it might appear disadvantageously redundant does provide a convenient and direct way of logically combining control signals generated by different processors or other elements so as to determine
15 maximums, minimums and the like. This lowers the circuit "overhead" associated with these techniques.

Whilst it is possible that there may be a one to one mapping between desired data processing performance level and an associated control signal, the present
20 abstraction technique conveniently supports many to one mappings as are often required due to the generally coarser level of control provided by the hardware relative to what can be specified by the software.

When operating a system using such many to one mapping, it is advantageous
25 that the control signals are quantised so as to support the maximum desired performance level that may be specified by the range of performance level request signal values mapped to the control signal value concerned. This ensures that minimum performance requirements are met as these are generally more critical than ensuring minimum energy consumption.

30

Preferred embodiments utilise a monotonic relationship between performance levels supported and control signal value with respect to performance level request signal value as this advantageously simplifies the programming of control of performance level.

As previously mentioned, the present techniques are well suited to operation across different clock domains.

5 The flexibility and reusability of the techniques may be enhanced by providing that at least one of the further circuits is configurable with configuration values specifying how the further circuit should respond to different control signal values. As an example of this, a voltage controller may be programmed with configuration values specifying voltage levels corresponding to different control signal values.
10 Thus, a voltage controller may be configured to match the circuit parameters of the rest of the system.

A strong advantage of the current technique is that it facilitates the provision of a system whereby while changing between performance levels the system is able to
15 operate at one or more intermediate performance levels prior to the final target performance level being reached. Thus, as compared with a system in which following a request to change to a higher performance level there is a relatively long latency until that performance level becomes available and is signalled as being available during which time the system operates at its original performance level, the
20 present technique allows the system to issue a request of its desired performance level and accept processing operation at any intermediate performance level which may be moved through prior to reaching the desired performance level. In many circumstances it may be that a request for an increased performance level is superseded before that increased performance level is finally reached, e.g. a high
25 priority interrupt indicating the need for a switch to maximum performance might in practice involve relatively little computation and thus be able to be serviced long before the switch to the highest performance level had been reached and so the request for the switch to the highest performance level could be cancelled with a consequent saving in energy.

30 A particularly good example of such intermediate performance level operation would be a change in the clock frequency which could step through one or more intermediate frequencies which would be utilised as they became available thus achieving the best forward progress thought the task concerned whilst awaiting the

target clock frequency to become available. Such clock frequencies may be unavailable pending availability of a suitable clock source signal or pending the voltage supply of the circuit reaching a level necessary to sustain processing operation at a higher clock frequency.

5

In preferred embodiments of the system, a priority signal (e.g. a "panic" signal) is able to override the program instruction control so as to trigger a change to a predetermined data processing performance level (e.g. maximum or reduced). This is advantageous from a design implementation point of view in providing hardware elements the ability to directly force performance changes in circumstances, such as interrupt handling or responding to a lower battery warning.

The management of performance level changes is improved in preferred embodiments in which the further circuits generate one or more current operation signals, giving information concerning their current operational state. This information can be fed to performance monitoring hardware and software in a manner that assists better performance management.

Strongly preferred examples of current operation signals include signals indicative of a maximum power supply voltage that can be supported by a voltage controller and a clock frequency currently being generated by a clock generator.

A clock generator may have one or more permanently available clock frequencies and for power saving reasons one or more selectively available clock frequencies, e.g. a permanently powered up PLL, providing frequencies including the minimum and maximum frequencies and a further PLL which may be temporally powered down for power saving reasons which serves to provide intermediate clock frequencies that are sometimes used.

In preferred embodiments of the invention, an increase in clock frequency is made when the necessary increased frequency clock signal is available and the voltage supply to the circuit is sufficient to support that increased frequency operation.

Viewed from another aspect the present invention provides a method of processing data, said method comprising the steps of:

performing data processing operations with a processor under control of program instructions, said processor being operable under program instruction control to generate a performance level request signal indicative of a desired data processing performance level of said processor; and

mapping with a mapping circuit said performance level request signal into a control signal supplied to one or more further circuits to control operation of said one or more further circuits so as to support said desired data processing performance level of said processor such that said program instructions controlling generation of said performance level request signal are independent of how said one or more further circuits are controlled to meet said desired data processing performance level.

Viewed from a further aspect the present invention provides a computer program product containing program instructions for controlling a processor, said program instructions comprising:

program instructions executable by said processor to set a desired data processing performance level to control one or more further circuits to support said desired data processing performance level operate, said desired data processing performance level having value linearly related to said desired data processing performance level.

Embodiments of the invention will now be described, by way of example only, with reference to the accompanying drawings in which:

Figure 1 schematically illustrates a portion of a data processing system including a performance controller, a clock generator and a voltage controller;

Figure 2 is a flow diagram schematically illustrating the operation of an operating system computer program in setting a desired performance level;

Figure 3 schematically illustrates an example mapping between desired performance level and control signal value;

Figure 4 is a flow diagram schematically illustrating the control of a voltage controller;

Figure 5 is a flow diagram schematically illustrating the control of a clock generator;

Figure 6 is a diagram schematically illustrating another example of a data processing system utilising the current techniques; and

Figure 7 is a diagram schematically illustrating a further example of a mapping between a desired performance level and a control signal value.

Figure 1 illustrates a portion of a data processing system including a performance controller 2, a clock generator 4 and a voltage controller 6. The circuits in Figure 1 typically form part of a larger integrated circuit which includes a processor, such as an ARM processor produced by ARM Limited of Cambridge, England, as well as other circuit elements, possibly as part of a system-on-chip design. The circuit elements other than the performance controller 2, the clock generator 4 and the voltage controller 6 are omitted from Figure 1 for the sake of simplicity. The performance controller 2 receives a performance level request signal/value which is generated under program instruction control by a computer program, such as an operating computer program, executing upon the processor (not illustrated). This desired data processing performance level request may be written to a dedicated memory location within the memory address space for such a purpose, may be written to a control register, such as a control register within a configuration coprocessor, e.g. CP15 ARM architecture or stored in some other way. The performance controller 2 also incorporates a performance monitor, which may be one or more performance counters counting the passage of real time, clock signals, work performed or other performance monitoring parameters. When the performance controller 2 receives a data processing performance level request indicative of a change in the desired performance level, then it is used issue a request for the new target clock speed to the clock generator 4 and a request for a new target voltage to the voltage controller 6. It will be appreciated that once the program instruction has written its desired data processing performance level to the appropriate location it

hands control of how that is put into effect to the hardware (performance controller 2). The performance controller 2 maps the desired data processing performance request to appropriate control signal values for the clock generator 4 and voltage controller 6 (the performance controller 2 includes a mapping circuit). The data processing performance request signal may be a Gray coded signal value or a simple linearly coded value. The mapping can be to a thermometer coded control signal value as this provides good resistance against sampling errors when sampling between clock domains which may be asynchronous. Furthermore, this provides a type of fail-safe behaviour whereby sampling errors tend to produce the lowest stable synchronised value for use.

The control signal passed to the voltage controller 6 instructs the voltage controller 6 to adopt a new voltage output level. The voltage output levels that are supported may be configured by programming configuration parameter registers 8 within the voltage controller 6 at bootup or some other time. The voltage controller 6 takes a finite amount of time to ramp up or down to the new voltage level. As it is changing to its new voltage level, the voltage controller 6 may pass through one or more intermediate levels which it would be capable of supporting an intermediate performance level pending reaching the final performance level. The voltage controller 6 generates current operation signals indicative of the current voltage levels it can support and passes these back to the performance controller 2 where they may be acted upon to trigger use of associated clock frequencies as appropriate and available.

The performance controller 2 also converts the desired data processing performance level specified by program control into control signals that are passed to the clock generator 4. These control signals specify a target clock frequency. The clock generator 4 is supplied with a variety of clock signals from one or more phase lock loop circuits 10, 12. One of these phase lock loop circuits 10 is permanently enabled and serves to provide the minimum and maximum clock frequencies supportable as well as some intermediate frequencies. Another of the phase lock loop circuits 12 is selectively available and can be powered down to save energy when the intermediate clock frequencies which it generates are not required.

The clock generator 4 generates a performance controller clock signal which is supplied to a technology dependent slack detector 14 within the voltage controller 6. This arrangement can be used to provide an additional level of control within the voltage controller 6 such that the voltage it is generating can be adjusted to support the target clock frequency with a reduced overshoot, i.e. the voltage level generated is just sufficient, with a small buffer, to support the target clock frequency. This fine level of control of the voltage output can be considered to be secondary to the gross performance level changes conducted in response to changes in desired data processing performance levels specified by program instructions. When a change to an increased performance level has been indicated, the voltage controller 6 will attempt to increase the voltage it is generating and when it is providing an increased voltage this is indicated back to the performance controller 2 which in turn can then control the CPU clock generator within the clock generator 4 to output a CPU clock signal cpuclock for supply to the processor having a new clock frequency sustainable with the new voltage, which may be an intermediate clock frequency on the way to the ultimate desired clock frequency. The clock generator 4 may not be capable of generating clock signals with the granularity that can be specified in the control signal values and accordingly passes back a quantised clock signal value corresponding to the actual clock frequency it is generating. Alternatively, this quantisation taking account of the actual capabilities of the clock generator 4 can take place within the mapping performed by the performance controller from the desired data processing performance request into the control signals.

Figure 2 schematically illustrates the processing operations which may be performed by an operating system computer program executing on a processor in accordance with one example of the technique. At step 16, the relevant processing thread waits until a determination is made of a need to change performance level. This need may be indicated by changes in external parameters, such as key presses by a user, or may be internally triggered through monitoring of the operational performance of the system using performance monitoring counters such as those previously discussed. When such a desired performance level change is detected, processing proceeds to step 18 at which the software performs a write to a memory mapped location dedicated to storing the desired data processing performance request level. The action of the computer program code is to detect the requirement for a

change in performance level and to write this requirement to a memory location. No control feedback need be provided to monitor that the desired change in performance actually takes place or how it takes place. There is an abstraction between the activity of the computer program in making this write and the underlying hardware mechanisms which act upon the request. This facilitates the use of substantially unaltered computer programs in a variety of environments taking advantage of whatever performance management mechanisms may or may not be provided within those environments.

Figure 3 schematically illustrates an example mapping between a 6-bit desired data processing performance request signal (which may optionally be Gray coded) and a corresponding thermometer coded control signal value. In this case whilst there are 33 possible performance levels, there are only 9 possible control signal values. Accordingly, there is a quantisation between the desired performance levels and control signal values. This quantisation is arranged such that the control signal value corresponds to the maximum performance level within a range of performance levels which may be mapped to that control signal value. There is a monotonic increase in the desired performance signal and the performance level this is intended to specify. Thus, the desired performance level can be a binary fraction representing a percentage of the maximum performance level that may be achievable in the system. This is a convenient and flexible way to abstract the performance level request in a manner which it can be controlled by program instructions in a wide variety of different hardware environments and for a wide variety of different processing purposes.

Figure 4 schematically illustrates control of the voltage controller 6. At step 20 the voltage controller waits for receipt of a new control signal. When a new control signal is received, processing proceeds to step 22 at which a change in the voltage level supplied is initiated. This change may be an increase or a decrease. The voltage controller 6 has a finite slew rate at which it can change its output. Step 24 monitors until the next sustainable voltage level is reached during the overall change which is occurring. When such a next level is reached, then step 26 is initiated and a new current voltage output signal is generated for supply back to the performance controller 2 to indicate the new voltage level which the voltage controller 6 is capable of supporting. This may be an intermediate voltage level on the way to the eventual

target voltage level, or at the end of the slew is the final target voltage level itself. The performance controller 2 can act upon this current voltage output signal fed back to it to control the clock generator and possibly the performance monitoring circuits. Step 28 determines whether the final voltage has yet been reached. If the final voltage
 5 has not yet been reached, then processing is returned to step 24 and slewing of the voltage output continues towards its eventual target.

It will be appreciated that Figure 4 assumes that the control signal does not change. In practice, the control signal may change before the final target voltage is
 10 reached. It may be that the need for a temporary change in performance level as determined by the program instructions within the operating system has gone away, such as an interrupt having been serviced or a panic mode signal having been de-asserted. In such circumstances, the control illustrated in Figure 4 is interrupted and processing returned to step 20 where action based upon the newly established control
 15 signal value is initiated. It will be appreciated that the control by the software is at least partially open loop in that it merely specifies which performance level it desires at a particular point in time but does not require monitoring of what performance is actually delivered or when the performance level is actually delivered.

20 As mentioned, a panic signal (priority signal or hardware override signal) may be supplied to the performance controller 2 to override any software control of the performance level and temporarily increase the performance level to a maximum level. Bypassing of the software control of performance level can facilitate more rapid and direct switching to maximum performance levels under purely hardware
 25 control, such as in response to specific high priority hardware interrupt signals. More than one such "panic" signal may be provided, e.g. a "Low-Battery-Panic" signal might force performance to a known reduced level.

Figure 5 schematically illustrates the control of the clock generator 4. At step
 30 30 the clock generator waits to receive a new control signal. When a new control signal is received, processing proceeds to step 32 at which a determination is made as to whether or not any additional phase lock loop circuit 12 needs to be powered up to service the ultimately required new clock frequency. If such additional phase lock

loop circuits 12 are required, then processing proceeds to step 34 where they are started. Alternatively, processing proceeds directly to step 36.

At step 36 the clock generator determines whether a new clock signal closer to
 5 the requested performance level is available. This facilitates the adoption of
 intermediate performance levels pending the availability of the eventual target
 performance level. When such an intermediate clock frequency is identified, then
 processing proceeds to step 38. Step 38 determines whether or not the current
 operation signal value fed back from the voltage controller 6 indicates that a voltage is
 10 being generated that is capable of sustaining the new clock signal value. When such a
 voltage is available, then processing proceeds to step 40 at which the new clock signal
 value is adopted and generated by the CPU clock generator as signal cpucclk which is
 supplied to the processor core. Step 42 then outputs a new current clock value back to
 the performance controller 2 where it may be acted upon by the performance
 15 monitoring hardware to assess the forward progress through the code. Step 44
 determines whether or not the switch to the new clock frequency has been the switch
 to the final clock frequency which was specified by the program instruction generated
 desired data processing performance request. If the final target clock frequency has
 not been reached, then processing returns to step 36, otherwise the control terminates,
 20 (effectively returns to step 30).

As for Figure 4, Figure 5 also assumes that the desired data processing
 performance level specified by the program instructions does not change. If this does
 change, then a new mapped control signal value will be generated which interrupts the
 25 processing illustrated in Figure 5 and returns the processing to step 30 whereupon the
 new control signal value is acted upon.

The adoption of intermediate clock frequency values whilst changing between
 an initial and a final clock frequency value allows the best forward progress through
 30 the code to be achieved for the particular state of the circuits concerned. The circuits
 do not stay operating at the initial clock frequency until the eventual target clock
 frequency becomes available, but instead ramp up or down through a sequence of
 clock frequencies as each becomes available during the performance slew. The
 adoption of a new clock frequency can be considered to be controlled by a logical

AND of a signal indicating that the frequency is closer to the target frequency than the current frequency, a signal indicating the availability of that frequency from a clock source together with a signal indicating that the voltage controller is capable of producing a power signal having a voltage sufficient to sustain operation at that new clock frequency.

Figure 6 is a diagram schematically illustrating a data processing system utilising the current techniques. Like elements to those illustrated in Figure 1 are given like reference numerals. Figure 6 additionally illustrates the processor 46 which executes the program instructions, which may be held within a tightly coupled memory system 48 or some other memory. The different voltage domains concerned necessitate level shifters to be provided at various interfaces in the circuit as illustrated.

Figure 7 illustrates another example mapping between desired data processing performance request level and thermometer coded control signal value. In this case a 32-bit thermometer coded control signal value is used yielding the possibility of a finer grained control of performance. It may be that the further circuits which respond to these 32-bit control signal values are in fact only capable of providing more coarsely grained control and so will effectively internally quantise the control signal values concerned. The thermometer coded control signal values provide a particularly convenient way of combining control signal values from different sources, such as from different processors on a multiprocessor system, whereby the overall performance level, which may be controllable only on a chip-wide basis, can be properly selected. A maximum control signal value can be determined by a logical OR of the control signal values, a minimum control signal value may be determined by a logical AND of the control signal value and equivalence may be determined by the XOR of the control signal values. The maximum function may be useful in determining the maximum requested clock frequency, the minimum function may be useful in indicating the minimum sustainable voltage and the equivalents function may be useful in determining a match between requirements of different elements.

CLAIMS

1. Apparatus for processing data, said apparatus comprising:
 - 5 a processor operable to perform data processing operations under control of program instructions, said processor being operable under program instruction control to generate a performance level request signal indicative of a desired data processing performance level of said processor; and
 - 10 a mapping circuit operable to map said performance level request signal into a control signal supplied to one or more further circuits to control operation of said one or more further circuits so as to support said desired data processing performance level of said processor such that said program instructions controlling generation of said performance level request signal are independent of how said one or more further circuits are controlled to meet said desired data processing performance level.
- 15 2. Apparatus as claimed in claim 1, wherein said one or more further circuits include a clock generator operable to generate a clock signal with a selectable clock frequency, said clock signal being supplied to said processor to drive said processing operations such that data processing performance of said processor varies in
20 dependence upon which clock frequency is selected.
3. Apparatus as claimed in any one of claims 1 and 2, wherein said one or more further circuits include a voltage controller operable to generate a power supply signal, said power supply signal being supplied to said processor at a selectable
25 voltage level, different voltage levels allowing different switching speeds within said processor such that a maximum usable data processing performance varies in dependence upon which voltage level is selected.
4. Apparatus as claimed in any one of the preceding claims, wherein said control
30 signal is a thermometer coded value.
5. Apparatus as claimed in claim 4, having a plurality of processors and mapping circuits operable to generate respective thermometer coded values which are logically

combined to produce a combined thermometer coded value to control at least one of said one or more further circuits.

6. Apparatus as claimed in any one of the preceding claims, wherein said mapping circuit performs a many to one mapping between performance level request signal values and corresponding control signal values.

7. Apparatus as claimed in claim 6, wherein said control signals are quantised such that a control signal value supports a maximum desired performance level within a range of desired performance levels having corresponding performance level request signal values mapped to said control signal value.

8. Apparatus as claimed in any one of the preceding claims, wherein performance level supported as controlled by control signal value increases monotonically with performance level request signal value.

9. Apparatus as claimed in any one of the preceding claims, wherein at least one of said one or more further circuits operates in a different clock domain to said processor.

10. Apparatus as claimed in any one of the preceding claims, wherein at least one of said one or more further circuits is configured with one or more configuration values specifying how said further circuit should respond to different control signal values.

11. Apparatus as claimed in claim 3 and claim 10, wherein said configuration values specify voltage levels corresponding to different control signal values.

12. Apparatus as claimed in any one of the preceding claims, wherein while responding to a change in performance control signal corresponding to a change from a first desired data processing performance level to a second desired data processing performance level, said one or more further circuits are operable to support data processing at at least one intermediate data processing performance level and said

processor temporarily operates at said at least one intermediate data processing performance level during said change.

13. Apparatus as claimed in claim 2, claim 3 and claim 12, wherein, in response to an increase in desired data processing performance level, said clock generator increases clock signal frequency to an intermediate clock signal frequency when said voltage controller is generating a power signal with a voltage level sufficient to support said intermediate clock signal frequency.

14. Apparatus as claimed in claim 12, wherein a priority signal serves to trigger said further circuit to change to support a predetermined data processing performance level independently of said performance control signal.

15. Apparatus as claimed in any one of the preceding claims, wherein at least while responding to a change in said performance control signal, said further circuit is operable to generate a current operation signal indicative of current operation of said further circuit.

16. Apparatus as claimed in claim 3 and claim 15, wherein said current operation signal is indicative of a maximum power supply voltage of that can currently be supported by said voltage controller.

17. Apparatus as claimed in claim 2 and claim 15, wherein said currently operation signal is indicative of a clock frequency that is currently being generated by said clock generator.

18. Apparatus as claimed in claim 2, wherein said clock generator is operable to generate a clock signal with one or more permanently available clock signal frequencies and one or more selectively available clock signal frequencies.

19. Apparatus as claimed in claim 18, wherein a permanently enabled PLL circuit is operable to generate said one or more permanently available clock signal frequencies and a selectively enabled PLL circuit is operable to generate said one or more selectively available clock signal frequencies.

20. Apparatus as claimed in claim 16 and any one of claims 17, 18 and 19, wherein, in response to an increase in desired data processing performance level, said clock generator increases clock signal frequency when said voltage controller
 5 generates a current operation signal indicative of a generation of said power signal with a voltage level sufficient to support an increased clock signal frequency.

21. A method of processing data, said method comprising the steps of:
 performing data processing operations with a processor under control of
 10 program instructions, said processor being operable under program instruction control to generate a performance level request signal indicative of a desired data processing performance level of said processor; and

mapping with a mapping circuit said performance level request signal into a control signal supplied to one or more further circuits to control operation of said one
 15 or more further circuits so as to support said desired data processing performance level of said processor such that said program instructions controlling generation of said performance level request signal are independent of how said one or more further circuits are controlled to meet said desired data processing performance level.

22. A method as claimed in claim 21, wherein said one or more further circuits include a clock generator operable to generate a clock signal with a selectable clock frequency, said clock signal being supplied to said processor to drive said processing operations such that data processing performance of said processor varies in dependence upon which clock frequency is selected.

23. A method as claimed in any one of claims 21 and 22, wherein said one or more further circuits include a voltage controller operable to generate a power supply signal, said power supply signal being supplied to said processor at a selectable voltage level, different voltage levels allowing different switching speeds within said
 30 processor such that a maximum usable data processing performance varies in dependence upon which voltage level is selected.

24. A method as claimed in any one claims 21, 22 and 23, wherein said control signal is a thermometer coded value.

25. A method as claimed in claim 24, wherein a plurality of processors and mapping circuits generate respective thermometer coded values which are logically combined to produce a combined thermometer coded value to control at least one of said one or more further circuits.

26. A method as claimed in any one claims 21 to 25, wherein said mapping is a many to one mapping between performance level request signal values and corresponding control signal values.

27. A method as claimed in claim 26, wherein said control signals are quantised such that a control signal value supports a maximum desired performance level within a range of desired performance levels having corresponding performance level request signal values mapped to said control signal value.

28. A method as claimed in any one of claims 21 to 27, wherein performance level supported as controlled by control signal value increases monotonically with performance level request signal value.

29. A method as claimed in any one of claims 21 to 28, wherein at least one of said one or more further circuits operates in a different clock domain to said processor.

30. A method as claimed in any one of claims 21 to 29, wherein at least one of said one or more further circuits is configured with one or more configuration values specifying how said further circuit should respond to different control signal values.

31. A method as claimed in claim 23 and claim 30, wherein said configuration values specify voltage levels corresponding to different control signal values.

32. A method as claimed in any one of claims 21 to 31, wherein while responding to a change in performance control signal corresponding to a change from a first desired data processing performance level to a second desired data processing performance level, said one or more further circuits are operable to support data

processing at at least one intermediate data processing performance level and said processor temporarily operates at said at least one intermediate data processing performance level during said change.

- 5 33. A method as claimed in claim 22, claim 23 and claim 32, wherein, in response to an increase in desired data processing performance level, said clock generator increases clock signal frequency to an intermediate clock signal frequency when said voltage controller is generating a power signal with a voltage level sufficient to support said intermediate clock signal frequency.

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34. A method as claimed in claim 32, wherein a priority signal serves to trigger said further circuit to change to support a predetermined data processing performance level independently of said performance control signal.

- 15 35. A method as claimed in any one of claims 21 to 34, wherein at least while responding to a change in said performance control signal, said further circuit is operable to generate a current operation signal indicative of current operation of said further circuit.

- 20 36. A method as claimed in claim 23 and claim 35, wherein said current operation signal is indicative of a maximum power supply voltage of that can currently be supported by said voltage controller.

- 25 37. A method as claimed in claim 22 and claim 35, wherein said currently operation signal is indicative of a clock frequency that is currently being generated by said clock generator.

- 30 38. A method as claimed in claim 22, wherein said clock generator is operable to generate a clock signal with one or more permanently available clock signal frequencies and one or more selectively available clock signal frequencies.

39. A method as claimed in claim 38, wherein a permanently enabled PLL circuit is operable to generate said one or more permanently available clock signal

frequencies and a selectively enabled PLL circuit is operable to generate said one or more selectively available clock signal frequencies.

40. A method as claimed in claim 36 and any one of claims 37, 38 and 39,
5 wherein, in response to an increase in desired data processing performance level, said clock generator increases clock signal frequency when said voltage controller generates a current operation signal indicative of a generation of said power signal with a voltage level sufficient to support an increased clock signal frequency.

10 41. A computer program product containing program instructions for controlling a processor to operate in accordance with the method as claimed in any one of claims 22 to 42.

42. A computer program product containing program instructions for controlling a
15 processor, said program instructions comprising:

program instructions executable by said processor to set a desired data processing performance level to control one or more further circuits to support said desired data processing performance level operate, said desired data processing performance level having value linearly related to said desired data processing
20 performance level.

43. A computer program product as claimed in claim 42, wherein said desired data processing performance level has a value equivalent to a binary fraction of a maximum data processing performance level.

ABSTRACT

DATA PROCESSING PERFORMANCE CONTROL

5 A processor 46 operating under program instruction control generates a
desired performance level request. A mapping circuit then maps this to a control
signal, such as a thermometer coded control signal, which is supplied to further
circuits which require control so as to support the desired data processing
performance level. These further circuits can include a clock generator 4 and a
voltage controller 6.

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[Figure 3]



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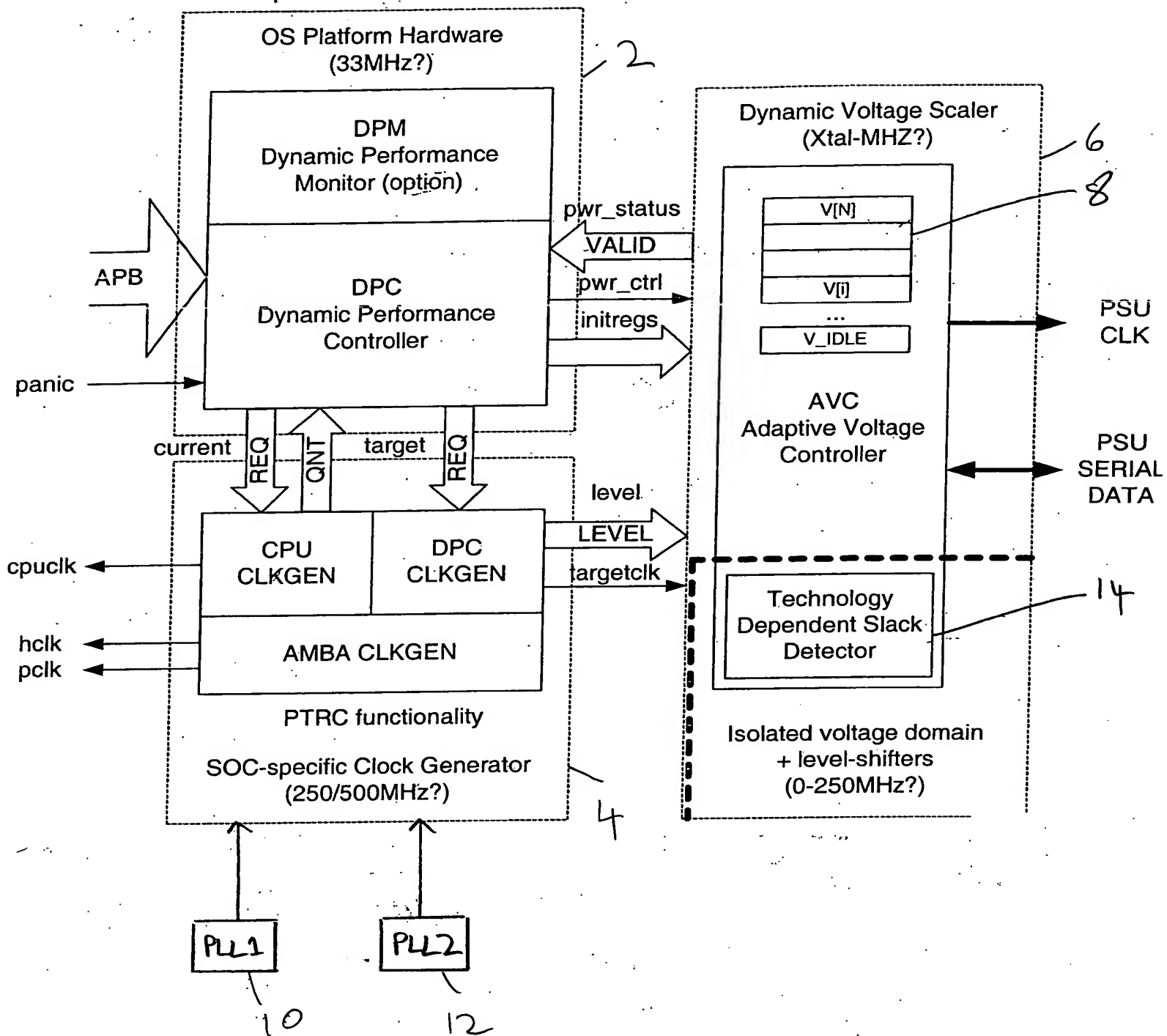


Fig. 1

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OS
Thread

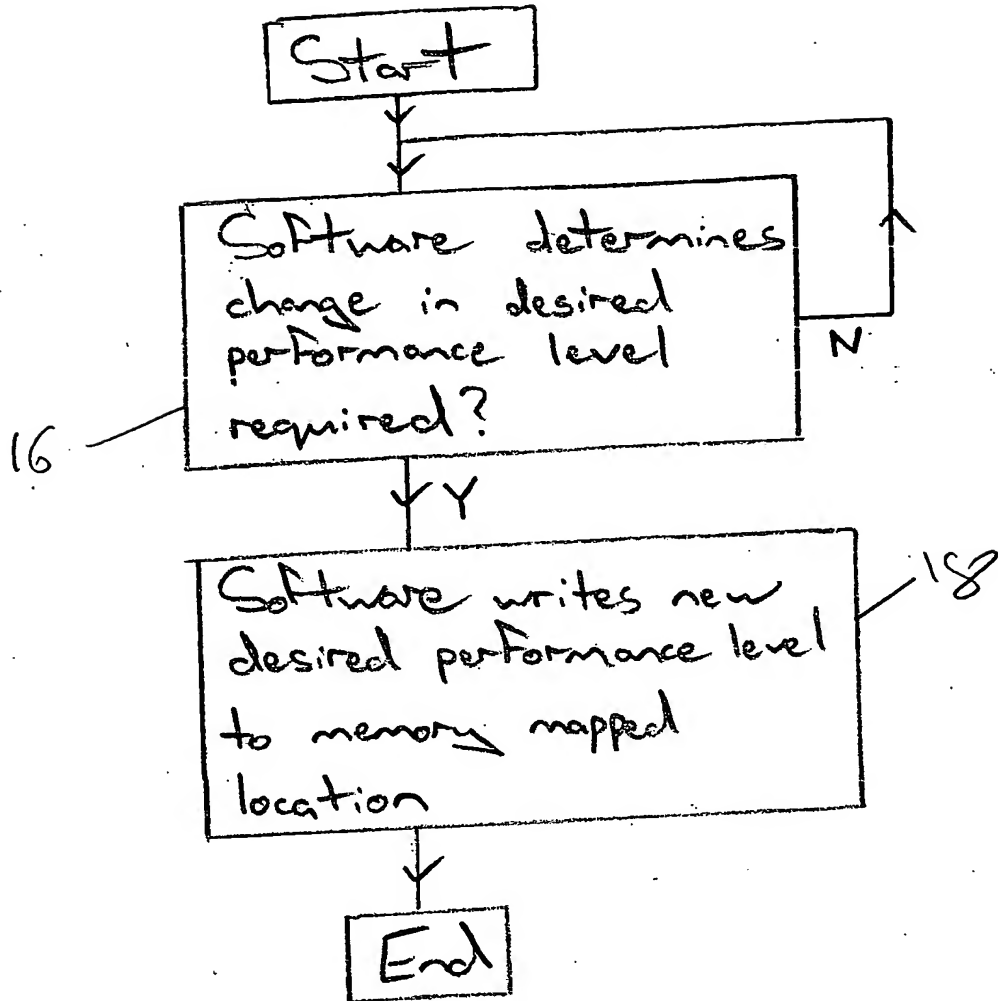


Fig. 2

Desired Performance
6-bit

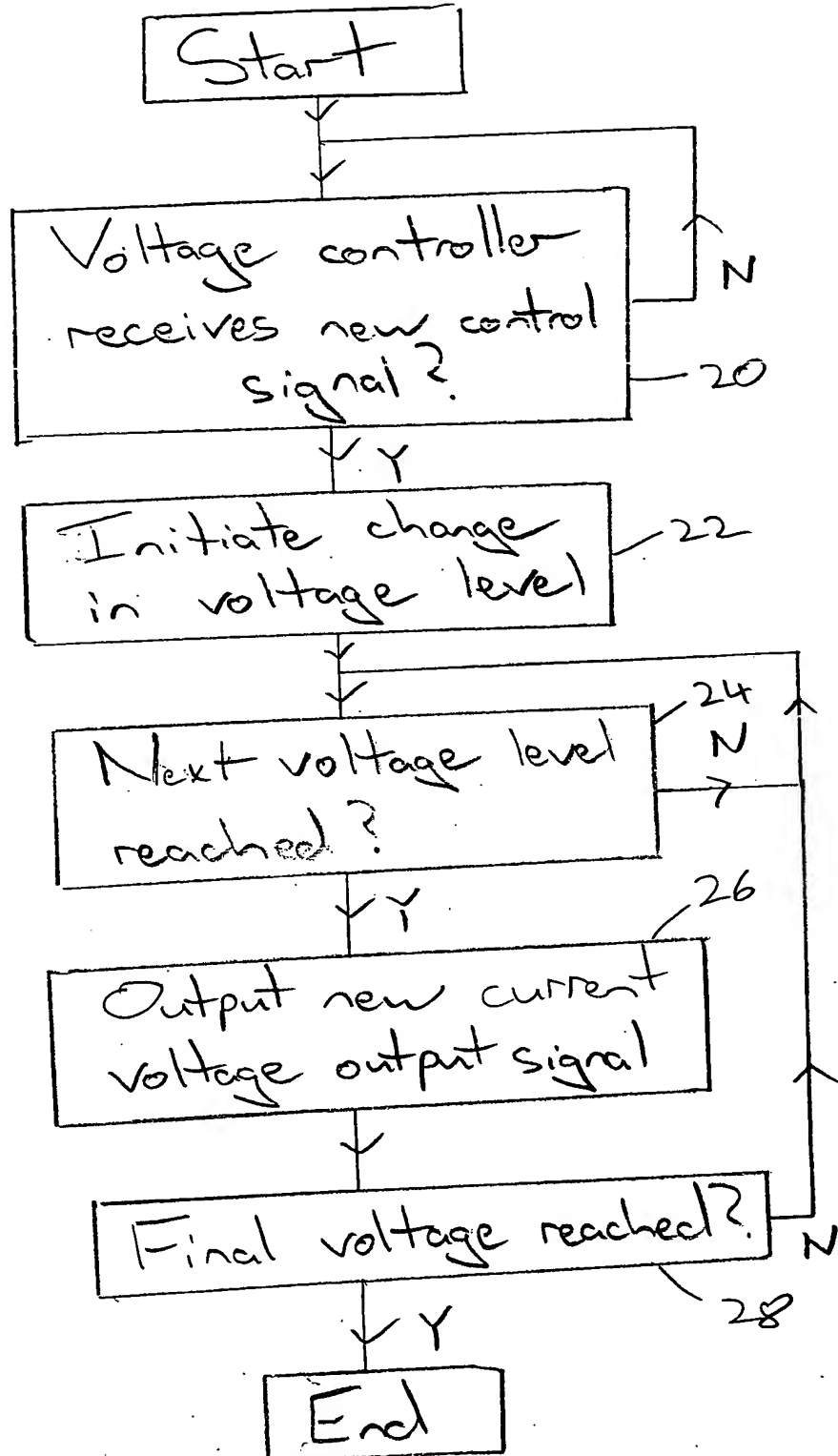
Control Signal
Value

0	00000000 Idle
1 - 4	00000001
5 - 8	00000011
9 - 12	00000111
13 - 16	00001111
17 - 20	00011111
21 - 24	00111111
25 - 28	01111111
29 - 32	11111111

Example Mapping

Fig. 3

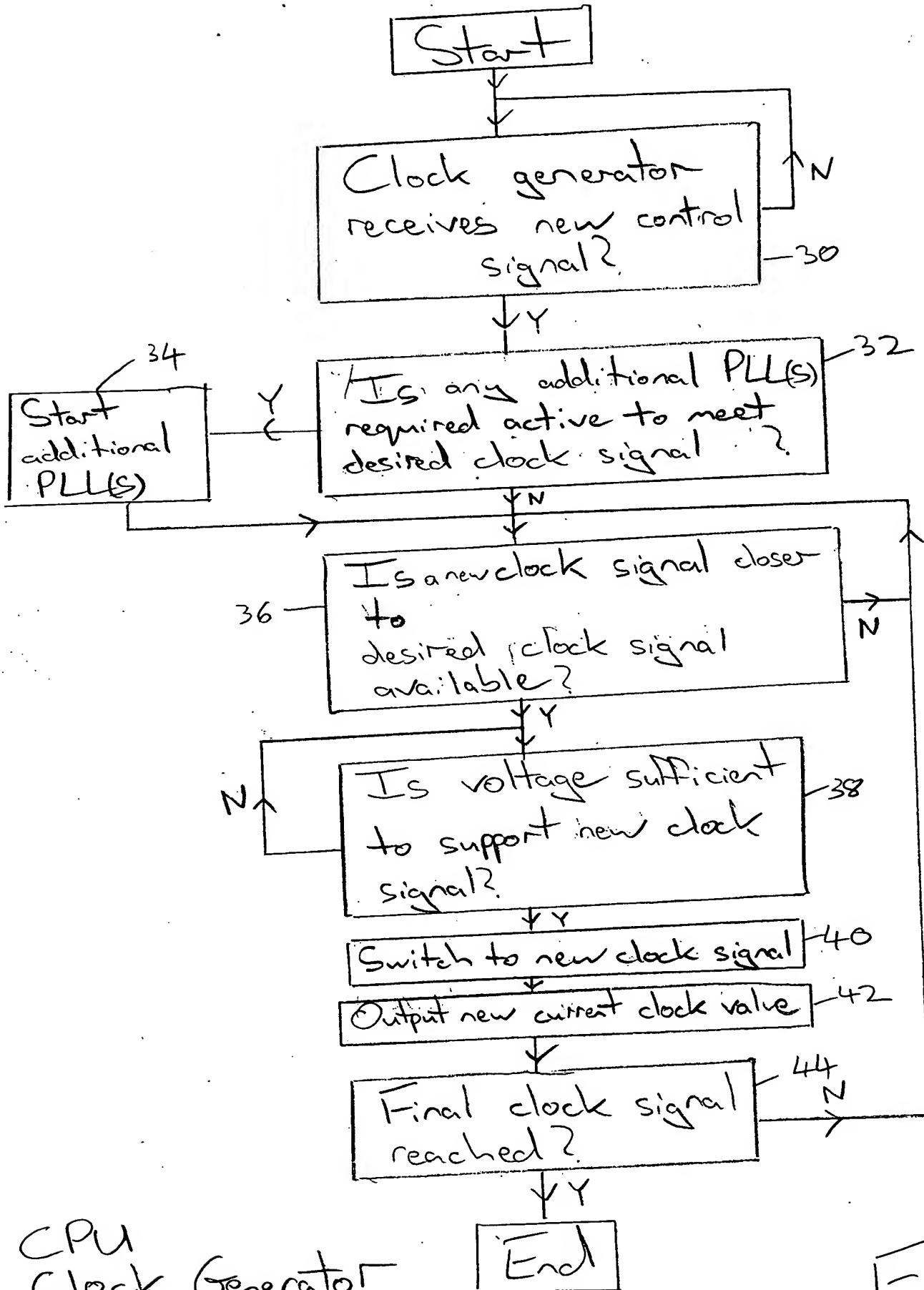
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Voltage Controller

Fig. 4

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CPU Clock Generator

Fig 5

717

Perf/32	Binary	Fractional	%	Coding	Note
32	1.00000	1.00000	100.0%	11111111111111111111111111111111	MAX
31	0.11111	0.96875	96.9%	01111111111111111111111111111111	
30	0.11110	0.93750	93.8%	00111111111111111111111111111111	
29	0.11101	0.90625	90.6%	00011111111111111111111111111111	
28	0.11100	0.87500	87.5%	00001111111111111111111111111111	
27	0.11011	0.84375	84.4%	00000111111111111111111111111111	
26	0.11010	0.81250	81.3%	00000011111111111111111111111111	
25	0.11001	0.78125	78.1%	00000001111111111111111111111111	
24	0.11000	0.75000	75.0%	00000000111111111111111111111111	
23	0.10111	0.71875	71.9%	00000000011111111111111111111111	
22	0.10110	0.68750	68.8%	00000000001111111111111111111111	
21	0.10101	0.65625	65.6%	00000000000111111111111111111111	
20	0.10100	0.62500	62.5%	00000000000011111111111111111111	
19	0.10011	0.59375	59.4%	00000000000001111111111111111111	
18	0.10010	0.56250	56.3%	00000000000000111111111111111111	
17	0.10001	0.53125	53.1%	00000000000000011111111111111111	
16	0.10000	0.50000	50.0%	00000000000000001111111111111111	
15	0.01111	0.46875	46.9%	00000000000000001111111111111111	
14	0.01110	0.43750	43.8%	00000000000000000111111111111111	
13	0.01101	0.40625	40.6%	00000000000000000011111111111111	
12	0.01100	0.37500	37.5%	00000000000000000001111111111111	
11	0.01011	0.34375	34.4%	00000000000000000000111111111111	
10	0.01010	0.31250	31.3%	00000000000000000000011111111111	
9	0.01001	0.28125	28.1%	00000000000000000000001111111111	
8	0.01000	0.25000	25.0%	00000000000000000000000111111111	
7	0.00111	0.21875	21.9%	00000000000000000000000011111111	
6	0.00110	0.18750	18.8%	00000000000000000000000001111111	
5	0.00101	0.15625	15.6%	00000000000000000000000000111111	
4	0.00100	0.12500	12.5%	00000000000000000000000000011111	
3	0.00011	0.09375	9.4%	00000000000000000000000000001111	
2	0.00010	0.06250	6.3%	00000000000000000000000000000111	
1	0.00001	0.03125	3.1%	00000000000000000000000000000001	
0	0.00000	0.00000	0.0%	00000000000000000000000000000000	IDLE

Figure 7.

